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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Kazuhiko OKAWA et al.

Application No.: 09/866,800

Filed: May 30, 2001 Docket No.: 109657

For: SEMICONDUCTOR DEVICE HAVING ELECTROSTATIC PROTECTION CIRCUIT AND METHOD OF FABRICATING THE SAME

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE SPECIFICATION:

Page 5, lines 22-27 and Page 6, lines 1-14 delete current paragraph and insert therefor:

According to one aspect of the present invention, there is provided a semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

Page 8, lines 7-27 and Page 9, lines 1-6 delete current paragraph and insert therefor:

A further aspect of the present invention provides a method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type well and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation

region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first

Page 12, lines 22-27 and Page 13, lines 1-14, delete current paragraph and insert therefor:

According to one embodiment of the present invention, there is provided a semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction

Page 20, lines 26-27 and Page 21, lines 1-25, delete current paragraph and insert therefor:

A further embodiment of the present invention provides a method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type well and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first

IN THE CLAIMS:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

24. (Amended) A method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type well and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.

REMARKS

Claims 1-24 are pending. By this Preliminary Amendment, the specification and claims are amended. Prompt and favorable examination on the merits is respectfully requested.

The attached Appendix includes marked-up copies of each rewritten paragraph (37 C.F.R. §1.121(b)(1)(iii)) and claim (37 C.F.R. §1.121(c)(1)(ii)).

Respectfully submitted,

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Attachment: Appendix

Date: September 26, 2001

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DEPOSIT ACCOUNT USE AUTHORIZATION
Please grant any extension necessary for entry;
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APPENDIX

Changes to Specification:

Page 5, lines 22-27 and Page 6, lines 1-14:

According to one aspect of the present invention, there is provided a semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the ~~N-type~~ MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

Page 8, lines 7-27 and page 9, lines 1-6:

A further aspect of the present invention provides a method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type wells and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.

Page 12, lines 22-27 and Page 13, lines 1-14:

According to one embodiment of the present invention, there is provided a semiconductor device comprising:

a semiconductor substrate;

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a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the ~~N-type~~ MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

Page 20, lines 26-27, Page 21, lines 1-25:

A further embodiment of the present invention provides a method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type wells and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation

region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (Amended) A semiconductor device comprising:

a semiconductor substrate;

a MOS transistor which is formed on the semiconductor substrate and includes a first diffusion region;

a first isolation region which isolates the MOS transistor from other MOS transistors on the semiconductor substrate;

a second isolation region formed between the ~~N-type~~ MOS transistor and the first isolation region;

a silicide layer formed on a surface of the semiconductor substrate excluding the first and second isolation regions;

a second diffusion region which is formed in a region isolated by the second isolation region and makes up a lateral bipolar transistor together with a well in the semiconductor substrate; and

a third diffusion region which is formed at a deeper position of the first diffusion region near the second isolation region and makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor.

24. (Amended) A method of fabricating a semiconductor device comprising the steps of:

forming a first isolation region which isolates a MOS transistor to be formed on a semiconductor substrate from other MOS transistors;

forming a second isolation region between the first isolation region and a region in which the MOS transistor is to be formed;

forming a P-type well and an N-type well in the semiconductor substrate;

forming a first diffusion region of the MOS transistor in a part of the P-type wells and the N-type well near the boundary of the P-type and N-type wells of the semiconductor substrate;

forming a second diffusion region which make up a lateral bipolar transistor together with one of the P-type well and the N-type well of the semiconductor substrate in a region isolated by the second isolation region;

forming a third diffusion region which makes up a Zener diode by the PN junction together with the first diffusion region of the MOS transistor, between the second isolation region and the first diffusion region and near a surface of the semiconductor substrate and; and

forming a silicide layer on a surface of the semiconductor substrate excluding the first and second isolation regions and a region connecting the first and third diffusion regions.